

## Advanced functional verification and debug of PCI Express-based designs

By Chris Browy

**V**erification Intellectual Property (VIP) streamlines the path to compliance sign-off through a reusable, layered verification methodology supported by highly configurable and feature-rich transactors, protocol assertions, advanced debug support, and comprehensive functional and compliance checklist test suites. Chris considers the role of VIP for core- and chip-level verification of PCI Express-based designs to ensure robust device-level and interface compliance.

### The challenge

Designing with today's high-speed serial interfaces such as PCI Express presents a more significant functional verification challenge than its predecessors, conventional PCI or PCI-X. Systems and peripherals using PCI Express interfaces can take advantage of Generation 1 and Generation 2 transfer rates, differentiated services such as quality of service, access control services, trusted configuration, active state power management, and advanced error reporting. However, these advanced features come at the expense of a more complex interface protocol, application logic, and software driver design.

This has given rise to a strong IP core market for PCI Express. Utilizing PCI Express logic core and PHY core design IP can significantly reduce the complexity of adding PCI Express support to chips and systems. This shifts the burden to the IP supplier for ensuring a rigorous verification of all the various core configurations before being considered trusted in any end-user design. Still, many of the advanced protocol features are substantially controlled through application logic and require custom tests to properly exercise the design functions.

The functional verification of PCI Express logic cores and the chips and systems utilizing them requires significant investment to develop and maintain a layered test bench environment comprised of transactors, assertions, test suites, and debug methods to isolate design bugs in different protocol layers. The test bench should be capable of core-through-chip verification including full control over the Device Under Verification's (DUV's) application logic interface as illustrated in Figure 1. Furthermore, the functional

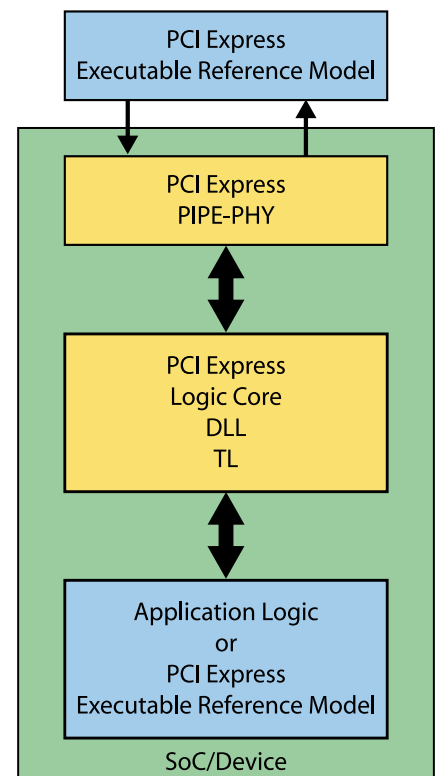


Figure 1

verification environment must constantly evolve to keep up-to-date with the latest specification errata and revisions. For example, since its initial release in 2003, the PCI Express standard has been revised several times, and major enhancements currently in the works signify that more changes will be made.

## Verification framework

A designer can choose from the following two options when performing the verification:

1. Develop their own test bench that will have its own inherent risks
2. Utilize an off-the-shelf test suite that has been proven through commercial use to provide the necessary verification coverage

Designers can then execute a comprehensive compliance validation test suite that exceeds basic compliance workshop requirements and supports advanced auto-debugging methods that isolate design bugs more effectively using a reference model and extensive protocol checkers.

A good verification solution should have a set of Executable Reference Models (ERMs) and test suites that simulate the behavior of any type of PCI Express and Advanced Switching (AS) components and links. The ERMs should be developed and presented as behavioral Verilog HDL source code models and augmented with a rich set of protocol assertions to provide the best verification. An ERM is between one to two orders of magnitude more efficient than implementation RTL in simulation.

DUVs should be verified against all realistic system topologies including simple crosslink, multihosted embedded systems, and switch-based topologies. All types of PCI Express Transaction Layer Packets (TLPs) and Data Link Layer Packets (DLLPs) should be generated. Robust controls over ERM operation at all protocol layers and back-end completion generation are needed. Host functions such as advanced PCI BIOS features including enumeration and device capability search must be supported as well as application-level features such as DMA.

The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. A test environment supporting Verilog, VHDL, SystemC, ANSI C/C++, Vera, SystemVerilog, Specman, and other programming environments can provide a native high-level API to interact with behavioral models supporting AS nodes, PCI Express root complexes, endpoints, switches, and PCI-X/PCI 2.3 devices.

A monitoring model that passively monitors and reports AS, PCI Express, and PCI/PCI-X protocol violations; validates end-to-end transactions; and measures and reports transaction trace analysis of devices by link bandwidth, latency,

routing, address, and command types utilized helps in the debugging process. A test environment that includes a full suite of compliance test scenarios that verify endpoint, switch, and bridge designs comply fully with the AS, PCI Express, and PCI/PCI-X specifications gives the maximum test coverage.

Compliance tests can be used to assist in the verification of each PCI Express component type and design. Portable tests with parameterized test sequence libraries supporting a rich set of transaction sequences for each of the PCI Express protocol layers and major functions best exercises the DUV. Test sequences are highly directed in nature and represent tens of months of work effort to cover all relevant scenarios. As shown in Figure 2, it is desirable to have test sequences that can be combined under directed or random modes to create a complete set of tests to verify a design against the expansive PCI-SIG compliance checklists. End users typically reuse test sequences to create custom device-level tests that meet their specific test needs.

## Bug detection and isolation methods

In response to these challenges, Avery Design Systems developed a complete verification framework for PCI Express that enables creating a highly accurate system model of a DUV in its system context.

An advancement in PCI Express verification over traditional verification methods, Avery's PCI-Xactor coverification has an ERM and innovative auto-debugging methods for bug detection and isolation. Using coverification the DUV and ERM run concurrently, applying the compliance and systems tests to both models. Transaction and sequential consistency is verified using preconfigured design match points, which track transaction flow between protocol layers of the DUV and ERM (see Figure 3). Architectural visible state and transactions are analyzed applying relaxed time, ordering, and content rules defined by the PCI Express protocol to ensure meaningful sequential consistency checking.

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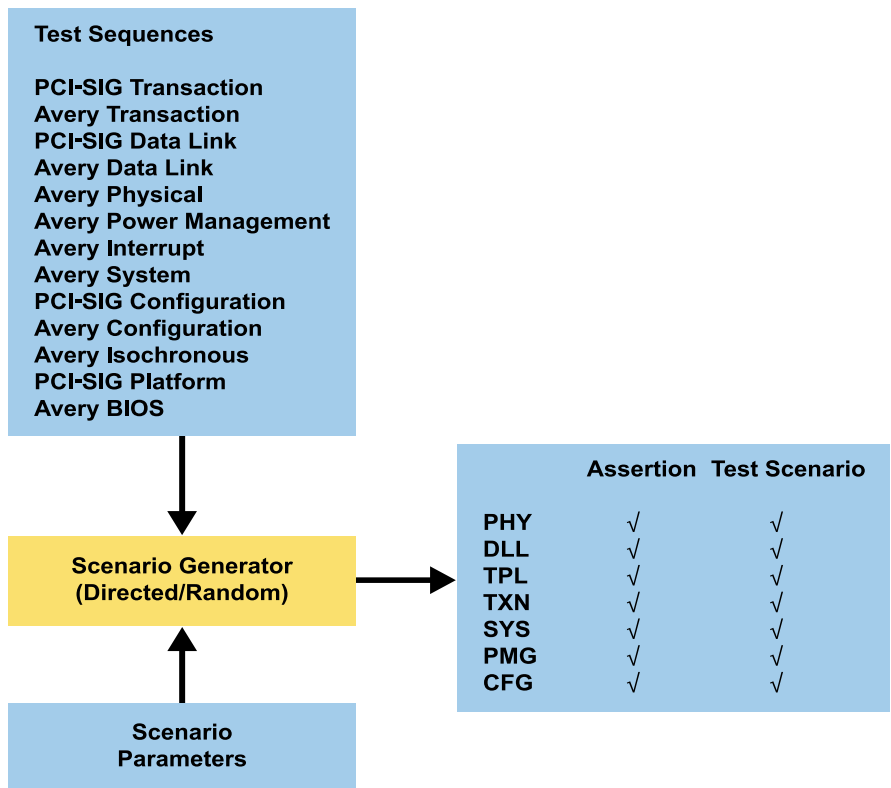


Figure 2

When a mismatch occurs, auto-debugging is then used to perform causal analysis of the implementation model and ERM. Auto-debugging utilizes enhanced behavior traversal and transaction views added to advanced behavioral debugging systems such as Novas' Verdi for better visualization of the behavior of the DUV and shadow ERM. Coverification is also especially useful in the context of random testing where expected device operation is too complex to predict or when assertions are too complex to write. Here, match points verify the architectural state of the models on-the-fly under random input sequences.

Some example of match points include:

- Link Training and Status State Machine (LTSSM) transitions
- Retry buffer entries and replay trigger
- VC flow credits counters
- Configuration and status registers

For example, Avery's design match capability isolated an incorrect LTSSM state transition to lower power state in a multifunction DUV under random test sequences.

### Embracing verification

Today, many systems companies and PCI Express logic core IP vendors are using advanced verification frameworks such as PCI-Xactor. Systems companies utilize core-level verification of logic and PHY cores in addition to complete device-level verification. **ECD**

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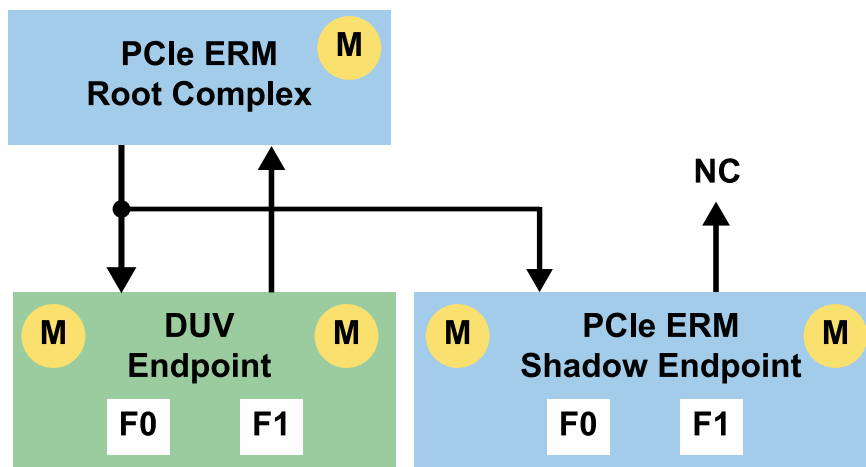


Figure 3